A Power-Efficient FPGA-Based Mixture-of-Gaussian (MoG) Background Subtraction for Full-HD Resolution

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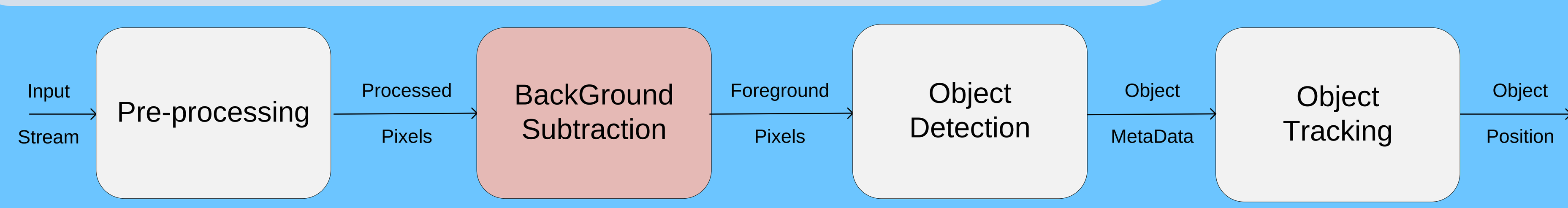
Mixture of Gaussians (MoG)

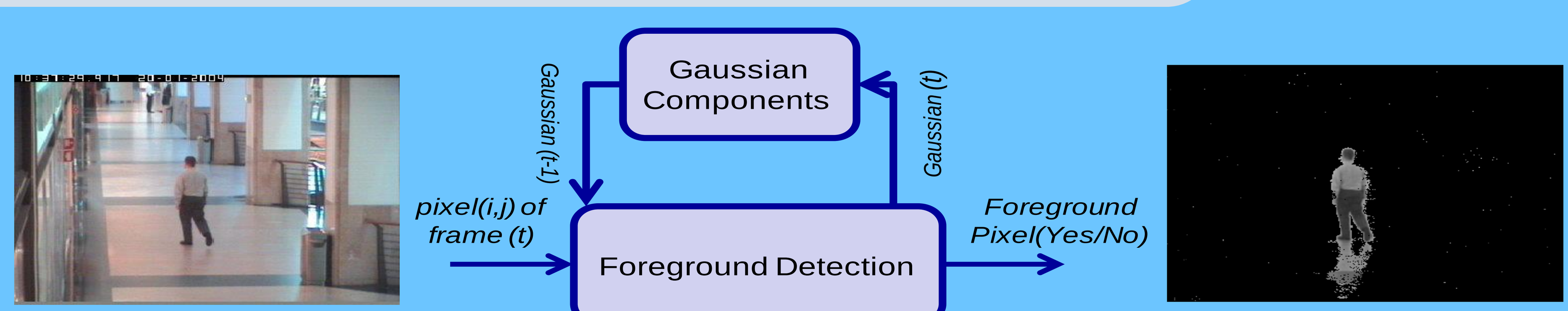
1) Background Subtraction

- Compute intense kernel early in vision flow
- Extracts ForeGround (FG) pixels from BackGround (BG) scene



2) Mixture of Gaussian (MoG)

- Adaptive learning-based BG tracking for static camera position



3) MoG Computation and Communication Demands

- 1080p60 in SW infeasible (24.3 GOPs)
  - 20 (float) or 13 (integer) Blackfin DSP)
- 32 bits per Gaussian parameters
  - (*weight, mean, standard deviation)*

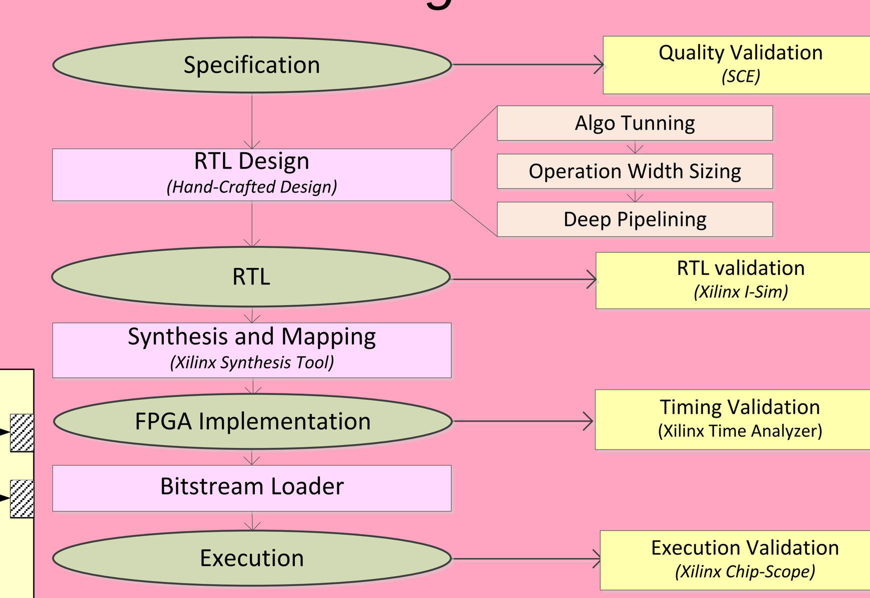
Image size	GOPs	Blackfin cores	Bandwidth [MB/Sec]	LPDDR2 Util.
1920*1080	24.3	13	7440	Saturated
1280*960	14.4	8	4380	70%

System Exploration

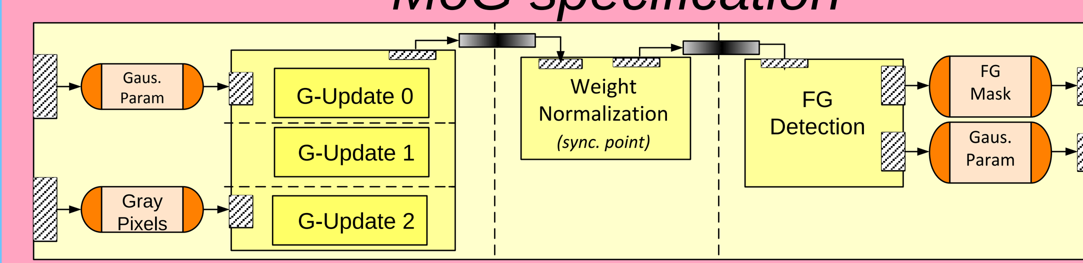
1) Design Flow

- Starting from system pacification
  - Captured in an SLDL
  - Coarse-grain parallelism

Design Flow

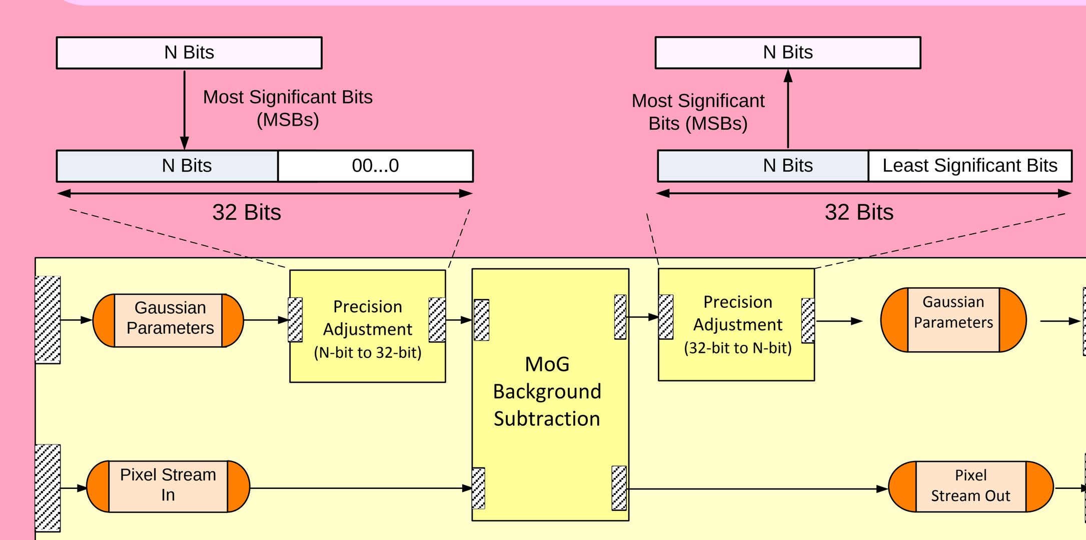


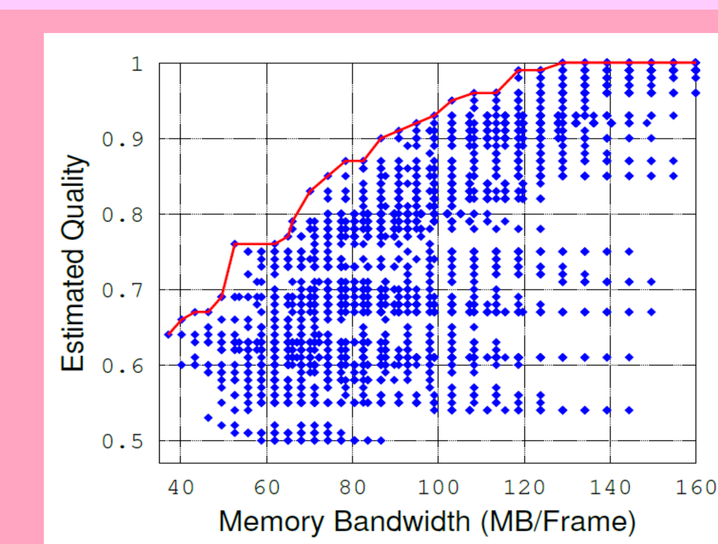
MoG specification



2) Parameter Precision, Bandwidth / Quality Trade-off

- Precision adjustment of Gaussian parameters
- Transfer/store only relevant bits of model
- Reduce bandwidth at cost of quality
- Quality assessment using MS-SSIM
  - PSNR less expressive
- Pareto front for selecting configuration, e.g.:
  - 95% quality at 63% bandwidth



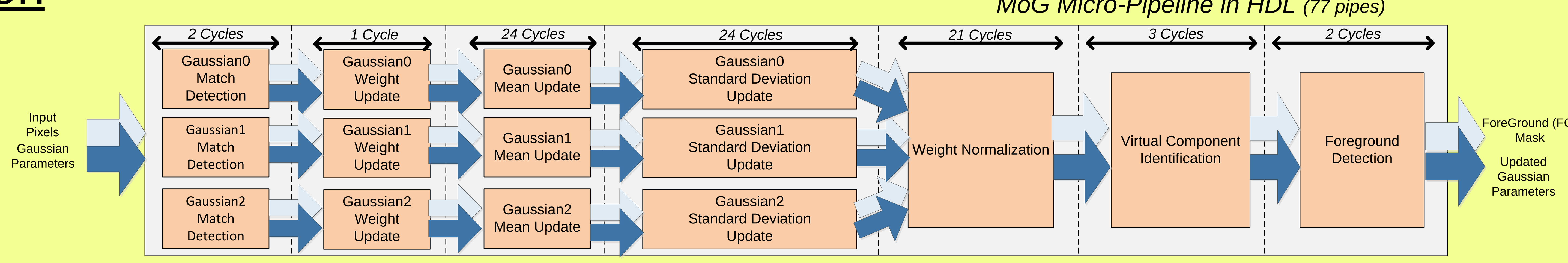


MoG Computation Realization

1) RTL Design

- Hand-crafted RTL implementation
  - Guided by system-level exploration / specification
- Full-HD (148.5 MHz)
- System pipeline (77 stages)
  - Macro pipeline (7 stages)

MoG Micro-Pipeline in HDL (77 pipes)

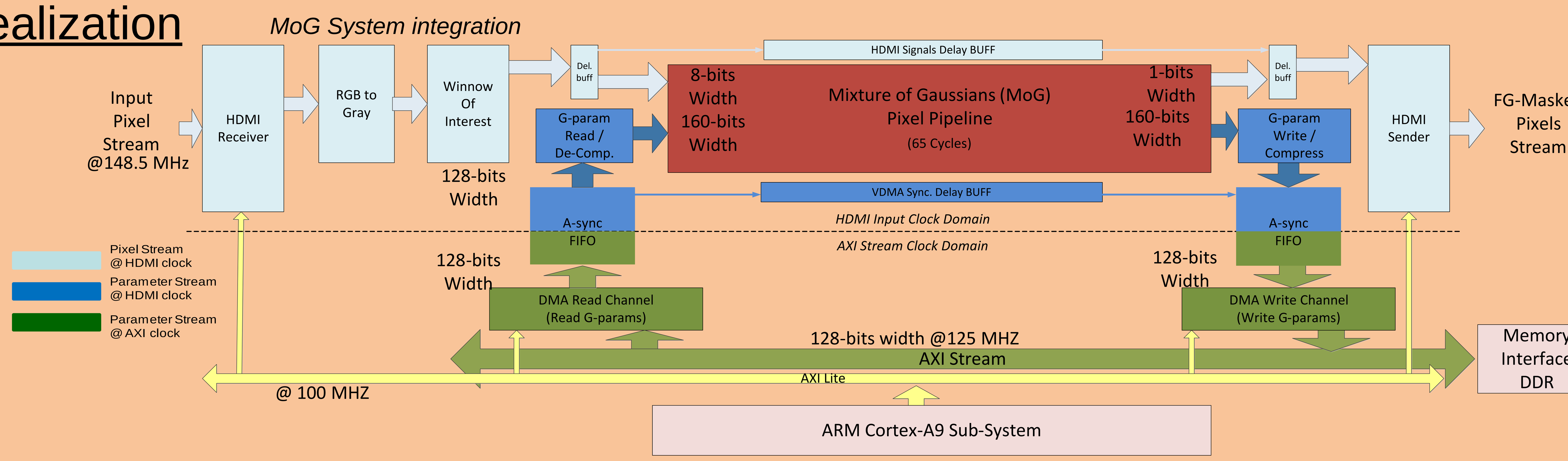


MoG Communication Realization

1) Communication Components

- Independent traffic management
  - Separate clock domains
- Dedicated Gaussian sizing unit
  - Transferring only important bits
- 2 DMA channels for Gaussian parameters
- Dedicated interconnect for burst transfer
- Async FIFOs
  - Bridge clock domains
  - Compensate for slow interconnect (148.5Mhz pixel v.s. 125Mhz bus)

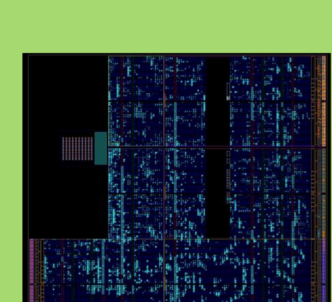
MoG System integration



Experimental Results

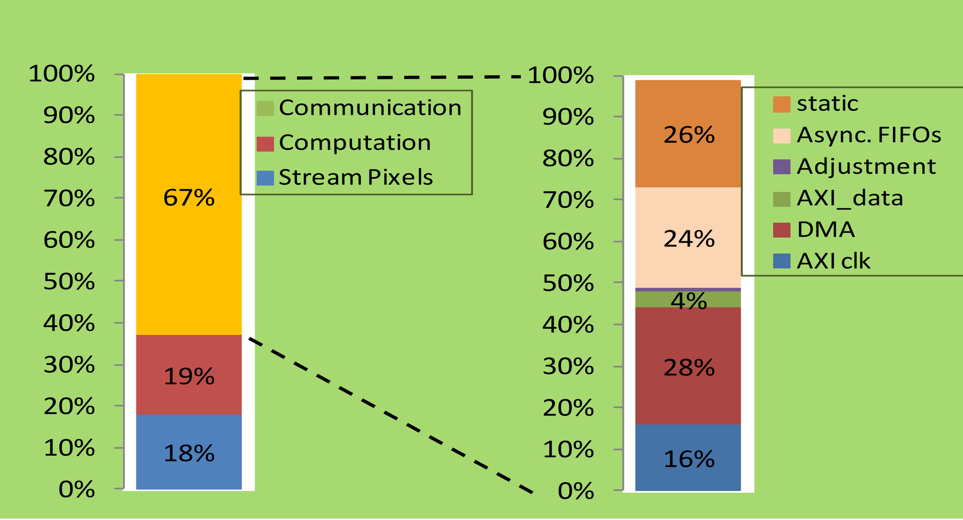
1) Zynq 7020 Realization

- Design spreads over chip
- Significant routing overhead
- 34% DSP slice utilization
- Resolution limited to 1080p @ 30FPs
  - Due to the Zynq peak memory bandwidth limitation: 4.2 GBs



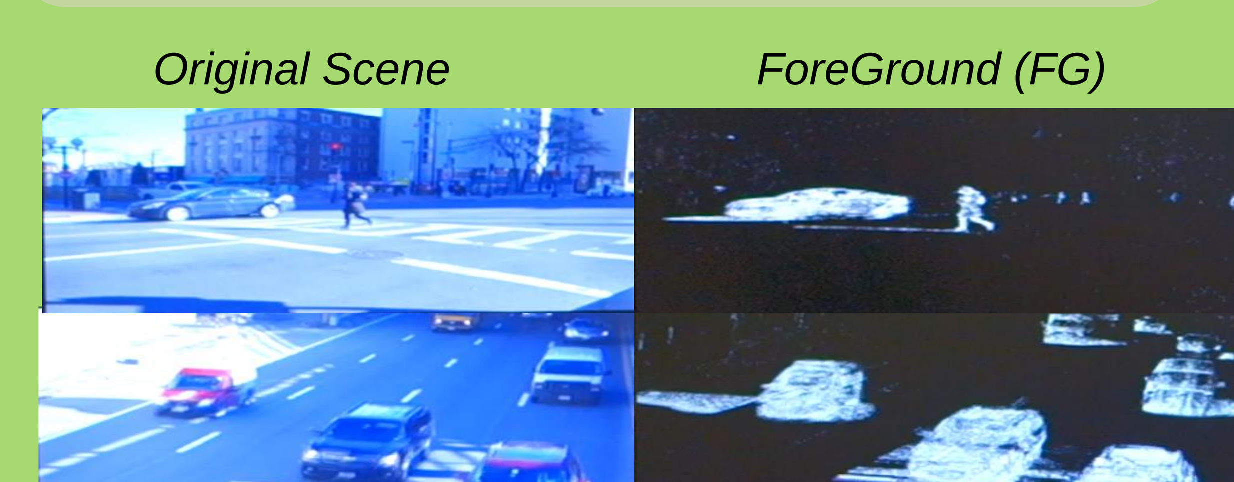
2) Power Consumption

- 600x more power efficient than SW (Cortex A9)
- 480mWatt on-chip power
  - Only 19% for computation
  - 67% for transferring Gaussian parameters



3) Functional Evaluation

- Correct FG detection for many scenes
  - Scenes with different complexity
    - Indoor/outdoor multiple moving objects
- >99% similarity [MS-SSIM] to specification model



Publication

- H. Tabkhi, R. Bushey, G. Schirner, "Algorithm and Architecture Co-Design of Mixture of Gaussian (MoG) Background Subtraction for Embedded Vision", Proceedings of the Asilomar Conference on Signals, Systems, and Computers (AsilomarSSC), Nov. 2013.