

# NASIBEH TEIMOURI

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## EDUCATION

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### Ph.D. Candidate, Electrical and Computer Engineering

Northeastern University, Boston, Massachusetts, USA

*Sep 2013–Dec 2017*

Thesis: Accelerator-based Chip Multi Processors (CMPs): Challenges and Solutions

GPA: 3.5/4

### Master of Science, Computer Engineering

Sharif University of Technology, Tehran, Iran

*Dec 2010*

Thesis: Reconfigurable Network on Chip (NoC): Energy and Performance Efficiency

GPA: 18.43/20

### Bachelor of Science, Computer Engineering

University of Tehran, Tehran, Iran

*Sep 2007*

Thesis: Parallel Realization of GSM Encoder through NoC

GPA: 15.39/20

## PROFESSIONAL SKILLS

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### Programming

- C/C++, Java, SpecC, SystemC, Verilog, VHDL, Matlab, C#, Cuda

### Scripting/ Markup Languages

- Python, Bash, Perl, PHP, Latex, HTML, XML, JavaScript, CSS

### Tools/Paradigms/Systems

- Object-oriented design, UML, Drupal, System on Chip Environment (SCE), Simulink, Statechart, GNU Parallel, Qt, SVN, Git

### Parallel programming

- Intel Threading Building Block (TBB), MPI, OpenMP

## RESEARCH INTERESTS

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System Level Design for Modeling, Test & Verification

Embedded Systems

Computer Architecture and Performance Analysis

## WORK EXPERIENCE

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Research Assistant at Massachusetts Open Cloud (MoC), Boston, MA, USA

*Sep 2017- Now*

- REST full API design for bare metal imaging (BMI) as one of active project in MoC.

Intern at Air WorldWide, Verisk, Boston, MA, USA

*Jan 2017- Jun 2017*

- High performance programming with Intel TBB, MPI and OpenMP for risk analysis software for insurance companies
- Performance analysis using Intel tools (Vtune, Inspector)

Research Assistant at Northeastern University, Boston, MA, USA

*May 2014- Aug 2017*

- Design and development of tools and architectures for accelerator-based chip multi-processors (CMPs)
- CMP modeling via SpecC programming language
- CMP model refinement and automatic virtual platform generation via the tool System on Chip Environment (SCE). System specification to test and implementation were automated using python script

Teacher Assistant at Northeastern University, Boston, MA, USA

*Sep 2014- Dec 2014*

- Embedded System Design: Enabling robotics. Students learn how to program Zedboard (both ARM processor and FPGA), work with the peripherals, and interface different actuators to the board. Finally they learn how to control a mechanical arm using Wiimote controller.

**Research Assistant at Northeastern University, Boston, MA, USA**

*Sep 2013- May 2014*

- Modeling performance estimation of Network on Chips (NoCs) using different levels of abstraction and estimation accuracy
- Implementation and test of NoC models in SpecC

**Website developer in Embedded System Laboratory (ESL) at Northeastern University, Boston, MA, USA**

*Sep 2013- Sep 2014*

- CMS/Druapl 7.x based website development
- Customization the website using PHP (hosted in www.neu.edu/esl)

**SW engineer at Informatics System Corporation (ISC) company, Tehran, Iran**

*Nov 2012- Jun 2013*

- Software development (C++ based) for ATM machine to assist disabled people

**Research Assistant at Sharif University of Technology, Tehran, Iran**

*Sep 2008- Apr 2012*

- Run-time reconfiguration of routers in NoC based on the application demand to improve energy and performance
- C++, Standard Template Library (STL), object oriented design principles, C#, and XML were heavily used in this project
- Developed a C++-based simulation platform to explore impacts of different scheduling algorithms on standby-sparing systems from energy/reliability trade-offs point of view

**Other projects**

*Sep 2005- Dec 2005*

- Developed a compiler for C-minus language in C++. Implemented all different steps to compile a code (parser, intermediate code generation, code generation, code optimization) from scratch.
- Critical-instruction aware cache replacement policy to enhance CPI. The SimpleScalar simulator was used in the project to detect critical instruction dynamically.
- Developed a framework to model fault injection in DRAM main memory with C++.
- Developed MPI implementation of network packet analyzer (the trace files were captured using Wireshark).
- Developed a 2D game using QT and C++
- Developed MIPS pipeline in FPGA using Verilog HDL

**TALKS**

**52<sup>nd</sup> DAC conference, SF, CA, USA**

*Jun 2015*

- Revisiting Accelerator-rich cmps: challenges and solutions

**Northeastern ECE PhD Student Association (NEPSA), Boston, MA, USA**

*Feb 2016*

- Improving Scalability of Chip-MultiProcessors with Many HW ACCElators

**PUBLICATIONS**

- Nasibeh Teimouri, et al. Understanding and resolving the scalability limitations of acc-based platforms. In **Transactions on Computer Aided Design (TCAD)**, 2017, under review.
- Nasibeh Teimouri, et al. Improving scalability of cmps with dense accs coverage. In **Design, Automation & Test in Europe (DATE)**, March 2016, 23% acceptance rate.
- Nasibeh Teimouri, et al. Revisiting accelerator-rich cmps: challenges and solutions. In **Design Automation Conference (DAC)**, June 2015, 29% acceptance rate.
- Ran hao, Nasibeh Teimouri, et al. Modeling and analysis of sldl-captured noc abstractions. In **International Embedded Systems Symposium (IESS)**, November 2015.

- Mohammad Khavari Tavana, Nasibeh Teimouri, et al. Simultaneous hardware and time redundancy with online task scheduling for low energy highly reliable standby-sparing system. In **ACM Transaction on Embedded Computing Systems (TECS)**, 2014, 24% acceptance rate.
- Mehdi Modarressi, Nasibeh Teimouri, et al. Improving the performance of packet-switched networks-on-chip by SDM-based adaptive shortcut paths. In **VLSI Integration**, 2015.
- Nasibeh Teimouri, et al. Power and performance efficient partial circuits in packet-switched networks-on-chip. In **International Conference on Parallel, Distributed, and Network-Based Processing (PDP)**, February 2013, 28% acceptance rate.
- Nasibeh Teimouri, Mehdi Modarressi, Arash Tavakkol, and Hamid Sarbazi-Azad. Energyoptimized on-chip networks using reconfigurable shortcut paths. In **Architecture of Computing Systems (ARCS)**, 2011.

## REFERENCES

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Dr. Gunar Schirner( <b>advisor</b> )	<a href="mailto:schirner@ece.neu.edu">schirner@ece.neu.edu</a>	<a href="http://www.ece.neu.edu/~schirner">http://www.ece.neu.edu/~schirner</a>
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