Embedded Systems Laboratory: Research Highlights

http://esl.coe.neu.edu

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Overview
The Embedded Systems Laboratory (ESL) is part of the Department of Electrical and Computer Engineering at Northeastern University, Boston, MA. It was established by Prof. Gunnar Schirner in 2009. Currently (summer 2014) 6 Ph.D., 8 M.S., and 3 undergraduate students enthusiastically research in the lab.

Main Research Interests
1) System-Level Design Automation
   - HW/SW codesign, modeling/simulation/analysis/synthesis
2) Cyber-Physical Systems (CPS) Design
   - Human involvement CPS / Domain Specific CPS
3) Novel Architectures Solutions for Embedded Vision
   - Computer vision and architectural complexity

Research Questions
- How to tame the functional and architectural design complexity?
- How to enable users to take benefit of massive parallelism and heterogeneous specializations in modern architectures?
- How to best match architecture and algorithm for an efficient embedded realization?

1) System-Level Design Automation
Integration of Simulink and System-Level Design

Simulink
- Algorithm simulation/verification/optimization
- System-Level Design
  - VP simulation/verification SYNTHESIZER
- Bridging the gap

Algo2Spec
- Synthesis (SystemC/
  SpecC) synthesis
- Structural Traceability
- Productivity Gain: 4X/2X

Algorithm/Architecture CoDesign Flow
- Unified flow
- New feedback loop for algorithm design
- Rapid estimation
- Performance + Traffic

Optimization Opportunity Example: Granularity / Efficiency Trade-off
- Many blocks/system design space
- Inefficient (e.g., no inter-block merging)
- Algo2Spec guided granularity selection based on computation and communication
- Over 12% model performance speedup (A2-MoG)

Challenges
- Manual implementation
- Time-consuming and Error-prone
- Requires Software and Hardware knowledge
- Current Synthesis Tools are Monolithic (either hardware or software)

Approach
- Super blocks for each processing element (PE)
- Insert proxies to emulate remote behavior
- Mix same inputs/output as replaced block
- Utilizes communication primitives from target processor
- E.g., memory mapped, registers, FIFOs
- Maintain synchronization across parallel executing processes

Publication (selected)
- "The Future of Human-Interactive Cyber Physical Systems," IEEE
- "Modernizing new Internet-by-Deployment," IEEE

2) Cyber-Physical Systems Design

Human-in-the-Loop Cyber-Physical Systems

Motivation
- Brain-Computer Interface (BCI): an interface between brains and computer systems, which enables effective technologies.
- BCI: eg. signal processing, intensive (MATLAB)

Objectives
- Establish a holistic design framework to integrate physical environment modeling providing an automated path from algorithm design to implementation
- Advance Body/Brain Computer Interface (BCBI) technology by incorporating accurate awareness, inference, and understanding under uncertain (such as navigation) and environmental conditions
- Design integratable, reliable and efficient real-time communication framework (integrating physically distributed components)

Transportation Infrastructure Performance Monitoring

Infrastructure Urban Challenges
- Societal need: Infrastructure Rate = 0
  - Non-normative: Traffic, gas, pollution, cost
  - Normative: Weather, city, nation-wide
- Deployable sensors/actuators
  - Frequent/Continuous Impact: Big Data
- Solution: CPS Meet Big Data

VOTERS Project
- Highly heterogeneous/expandable
  - Three-tier design
  - 20 heterogeneous sensors
  - 20,000,000,000 ultrasound events, 1 day
  - Service and critically aware
  - Deployed to a van
  - Inspection at city level
  - Fully automated flow

Challenges
- Complex algorithms
- Diversity of sensors
- High res. (103bps) and rate (8Gbps)
- Significant correlation
  - 50 GOPS – 100 GOPS
- Huge bandwidth
  - 8–10 Gbps
- Very low power
  - Less than 1 W

Current Approaches
- Focus on pre-processing (Waves)
- Multi-processing stuck on I/O
- Flexible, but inefficient

Future
- Explainability
- Simplicity
- Analyzability
- Portability
- Security

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3) Novel Solutions for Embedded Vision

Efficient Solutions for Adaptive Streaming Kernels

Communication-Centric Architecture Template
- Independent management for streaming and algorithms
- Dynamic data
- Precision adjustment
- Quality vs. bandwidth

Zynq Prototype
- Target: 1080p at 30fps
- Mixture of Gaussian (MoG)
- Background subtraction
  - 480x640 at on-chip power
  - 5X less power than Cortex A8

Publication (selected)
- "Non-adaptive object detection: Capabilities and limitations," IEEE

Function Level Processor (FLP)

Goals
- Bridge flexibility / efficiency
- Architecting @ function-level to increase efficiency / human flexibility
- Market-oriented / domain-specific

Approach
- Group functionality into compilable Function Blocks (FB)
- Customized FB interconnected
- Chain FBs to macro pipeline
- Autonomous control and sync
- Minimize host I/O interaction

Results
- 10-20% less power than an LP
- > 5x less power than an LP-HWACC

Funding Sources
- NIST
- Analog Devices
- MathWorks
- David Rose Foundation
- MGIIP