Hamed Tabkhi

Contact Information

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Electrical and Computer Engineering
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Education

Ph.D. in Electrical and Computer Engineering *09/2010 - 09/2014*
Northeastern University, Boston, MA, USA
- Dissertation title: High-performance power-efficient solutions for embedded vision computing
- Supported by Analog Devices Inc. (ADI) with a $125K grant
- Advisor: Prof. Gunar Schirner

M.Sc. in Computer Engineering *09/2006 - 09/2008*
Sharif University of Technology, Tehran, Iran
- Thesis title: Design and evaluation of low-power error detection and roll back recovery
- Advisor: Prof. S.G. Miremadi

Research Positions

Post-Doctoral Research Scientist *10/2015 – Present*
Northeastern University, Boston, MA, USA
- Leading embedded architecture team to architect and prototype novel heterogeneous many-core solutions for real-time embedded vision processing
- Flexible function-level accelerators for streaming applications
- Understanding the OpenCL parallelism semantic on FPGA devices
- Power-efficient architecture for real-time Deep Neural Network (DNN) processing
- Supervising 3 Ph.D. and 5 M.Sc. students
- Preparing federal grant proposals (as a Co-PI)

Post-Doctoral Research Associate *10/2014 – 10/2015*
Northeastern University, Boston, MA, USA
- Designed and architected accelerator-based many-core platforms for streaming applications
- Defined WPS as a metric to capture and analyze thread-level execution similarity on GPUs
- Studied the efficiency of GPUs and FPGAs for irregular data-intensive applications
- Supervised 2 Ph.D. and 3 M.Sc. students

Ph.D. Research Assistantship *09/2010 – 09/2014*
Northeastern University, Boston, MA, USA
- Joint collaboration with **Analog Devices Inc. (ADI)**, direct collaborator: Robert Bushey, principle technologist/architect, now with Intel
- Designed and architected a novel processor class: Function-Level Processor (FLP) to break free architecture flexibility and efficiency
- Architected and prototyped a real-time object tracking vision flow on Xilinx Zynq platform
- Proposed a design methodology: Conceptual Abstraction Levels (CALs) to manage architecture complexity of market-oriented MPSoCs
- Developed a cross-layer approach to enhance the energy-efficiency and reliability of DSPs
- Designed and developed a SystemC-based Instruction-Set Simulator (ISS) for Blackfin DSPs

M.Sc. Research Assistantship *09/2006 – 09/2008*
Sharif University of Technology, Tehran, Iran
- Designed and modeled schemes for power-efficient reliable on-chip data communication
- Proposed a power-efficient error detection and recovery scheme for embedded processors

Publications

** indicates students under my supervision*

Peer-Reviewed Journal Articles

J8. C. Zhang*, **H. Tabkhi** and G. Schirner, "Studying Inter-Warp Divergence Aware Execution on GPUs", IEEE *Computer Architecture Letters*, in Press (accepted in 09/03/2015).

J7. **H. Tabkhi**, R. Bushey and G. Schirner, "Function-Level Processor (FLP): A Novel Processor Class for Efficient Processing of Streaming Applications", S*pringer Journal of Signal Processing and Systems*, in Press (accepted in 09/21/2015).

J6. **H. Tabkhi**, R. Bushey and G. Schirner, "Conceptual Abstraction Levels (CALs) for Managing Design Complexity of Market-Oriented MPSoCs", Elsevier Journal of Microprocessors and Microsystems, vol.39, no.8, pp. 704-719, Nov. 2015.

J5. **H. Tabkhi** and G. Schirner, "A Joint SW/HW Approach for Reducing Register File Vulnerability", *ACM Transactions on Architecture and Code Optimization (ACM TACO)*, vol.12, no.2, pp.1-28, May. 2015.

J4. **H. Tabkhi**, M. Sabbagh and G. Schirner, "A Power-Efficient Real-Time Solution for Adaptive Vision Algorithms", *IET Computers & Digital Techniques*, vol.9, no.1, pp.16-26, Jan. 2015.

J3. **H. Tabkhi**, R. Bushey and G. Schirner, "Function-Level Processor (FLP): A High Performance, Minimal Bandwidth, Low Power Architecture for Market-Oriented MPSoCs", *IEEE Embedded Systems Letters*, vol.6, no.4, pp.65-68, Dec. 2014.

J2. **H. Tabkhi** and G. Schirner, "Application-Guided Power Gating Reducing Register File Static Power", *IEEE Transactions on Very Large Scale Integration (TVLSI)*, vol.22, no.12, pp.2513-2526, Dec. 2014.

J1. A. Patooghy, G. S Miremadi and **H. Tabkhi**, "A Reliable and Power Efficient Flow-Control Method to Eliminate Crosstalk Faults in Network-on-Chips", *Microprocessors and Microsystems - Embedded Hardware Design*, vol 35, no. 8, pp. 766-778, Nov. 2011.

Peer-Reviewed Conference Papers

C18. **H. Tabkhi**, M. Sabbagh* and G. Schirner, "Guiding Power/Quality Exploration for Communication-Intense Stream Processing" Great Lakes Symposium on VLSI (GLS-VLSI), Boston (MA), USA, May 2016.

C17. N. Teimouri*, **H. Tabkhi** and G. Schirner, "Improving Scalability of CMPs with Dense ACCs Coverage", *IEEE Design Automation and Test in Europe (DATE)*, Dresden, Germany, Mar. 2016.

C16. M. Sabbagh*, **H. Tabkhi** and G. Schirner, "Taming the Memory Demand Complexity of Adaptive Vision Algorithms", *IFIP International Embedded Systems Symposium (IESS)*, Foz do Iguacu, Brazil, Nov. 2015.

C15. **H. Tabkhi**, M. Sabbagh* and G. Schirner, "An Efficient Architecture Solution for Low-Power Real-Time Background Subtraction", *IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP)*, Toronto, Canada, Jul. 2015.

C14. A. Momeni*, **H. Tabkhi**, Y. Ukidave, G. Schirner and D. Kaeli, "Exploring the Efficiency of the OpenCL Pipe Semantic on an FPGA", *International Symposium on Highly Efficient Accelerators and Reconfigurable Technologies (HEART)*, Boston (MA), USA, Jun. 2015.

C13. N. Teimouri*, **H. Tabkhi** and G. Schirner, "Revisiting Accelerator-Rich CMPs: Challenges and Solutions", *ACM/EDAC/IEEE Design Automation Conference (DAC)*, San Francisco (CA), USA, Jun. 2015.

C12. Ch. Zhang*, **H. Tabkhi** and G. Schirner, "A GPU-based Algorithm-specific Optimization for High-performance Background Subtraction", *International Conference on Parallel Processing (ICPP)*, Minneapolis (MN), USA, Sep. 2014.

C11. **H. Tabkhi**, R. Bushey and G. Schirner, "Function-Level Processor (FLP): Raising Efficiency by Operating at Function Granularity for Market-Oriented MPSoCs", *IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP)*, Zurich, Switzerland, Jun. 2014 (best paper runner-up).

C10. **H. Tabkhi**, R. Bushey and G. Schirner, "Algorithm and Architecture Co-Design of Mixture of Gaussian (MoG) Background Subtraction for Embedded Vision", *IEEE Asilomar Conference on Signals, Systems, and Computers (AsilomarSSC)*, Monterey (CA), USA, Nov. 2013.

C9. R. Bushey, **H. Tabkhi** and G. Schirner, "Flexible Function-Level Acceleration of Embedded Vision Applications using the Pipelined Vision Processor", *IEEE Asilomar Conference on Signals, Systems, and Computers (AsilomarSSC)*, Monterey (CA), USA, Nov. 2013 (invited).

C8. R. Bushey, **H. Tabkhi** and G. Schirner, "A Novel Quantitative ESL Based SOC Architecture Exploration Methodology", *Analog Devices General Technical Conference (ADI GTC)*, Apr. 2013 (industry conference).

C7. **H. Tabkhi** and G. Schirner, "AFReP: Application-guided Function-level Registerfile Power-gating for Embedded Processors", IEEE/ACM *International Conference on Computer-Aided Design (ICCAD)*, San Jose (CA), USA, Nov. 2012.

C6. **H. Tabkhi** and G. Schirner, "ARRA: Application-guided Reliability-enhanced Registerfile Architecture for Embedded Processors", *IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC)*, Santa Cruz (CA), USA, Oct. 2012.

C5. **H. Tabkhi** and G. Schirner, "Application-Specific Power-Efficient Approach for Reducing Register File Vulnerability", *IEEE Design Automation and Test in Europe (DATE)*, Dresden, Germany, Mar. 2012.

C4. A. Patooghy, **H. Tabkhi** and G. S Miremadi, "An Efficient Method to Reliable Data Transmission in Network-on-Chips", *Euromicro Conference on Digital System Design: Architectures, Methods and Tools (DSD)*, Lille, France, Sep. 2010.

C3. A. Patooghy, **H. Tabkhi** and G. S Miremadi, "RMAP: A Reliability-Aware Application Mapping for Network-on-Chips", *International Conference on Dependability (DEPEND)*, Venice/Mestre, Italy, Jul. 2010.

C2. H. Ghasemzadeh-Mohammadi, **H. Tabkhi**, G. S Miremadi and A. Ejlali, "A cost-effective error detection and roll-back recovery technique for embedded microprocessor control logic", *IEEE International Conference on Microelectronics (ICM)*, Sharjah, United Arab Emirates, Dec. 2008.

C1. **H. Tabkhi**, G. S Miremadi and A. Ejlali, "An Asymmetric Checkpointing and Rollback Error Recovery Scheme for Embedded Processors", *IEEE International Symposium on Defect and Fault Tolerance of VLSI Systems (DFT)*, Cambridge (MA), USA, Oct. 2008.

Workshop Papers / Conference Poster Abstracts

WP3. A. Momeni*, **H. Tabkhi**, G. Schirner and D. Kaeli, "OpenCL-based Optimizations for Acceleration of Object Tracking on FPGAs and GPUs", *International Workshop on Architectures and Systems for Real-time Mobile Vision Applications (ASR-MOV), in Conjunction with CGO'16*, Barcelona, Spain, 12 Mar. 2016.

WP2. A. Momeni*, **H. Tabkhi**, G. Schirner and D. R. Kaeli, "Bridging Architecture and Programming for Throughput-Oriented Vision Processing", *International Symposium on Field-Programmable Gate Arrays (FPGA)*, Monterey (CA), USA, Feb. 2015.

WP1. **H. Tabkhi**, M. Sabbagh* and G. Schirner, "A Power-efficient FPGA-based Mixture-of-Gaussian (MoG) Background Subtraction for Full-HD Resolution", *IEEE International Symposium on Field-Programmable Custom Computing Machines (FCCM)*, Boston (MA), May 2014.

Journal Articles under Submission

JS2. A. Momeni*, **H. Tabkhi**, G. Schirner and D. Kaeli, "Understanding the OpenCL Parallelism Semantic on FPGA Devices", *targeted for ACM Transactions on Architecture and Code Optimization (ACM TACO).*

JS1. N. Teimouri*, **H. Tabkhi** and G. Schirner, "Transparent Self-Synchronized (TSS) Architecture to Remove Scalability Limitations of Accelerator-Rich CMPs", targeted for *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (T-CAD).*

Teaching Experience

Guest Lecturer, "Microprocessor-Based Design" *01/2016-Present*
ECE department, Northeastern University, Boston, MA, USA
- Teaching principles of HW/SW co-design based on Xilinx Zynq platform

Instructor/Lecturer, "Enabling Embedded Robotics" *09/2015-12/2015*
ECE department, Northeastern University, Boston, MA, USA
- Taught and designed a novel course covers fundamentals of computer engineering
- Students engaged in a practical learning process to program Xilinx Zynq platforms for controlling a robot (over 30 students)
- Received a very good student evaluation (4.1 out of 5.0 for teaching effectiveness)

Guest Lecturer, "High-Level Design of Hardware / Software Systems" *10/2015-12/2015*
ECE department, Northeastern University, Boston, MA, USA
- Lectured on the system-level re-targetable performance estimation approaches

Instructor/Lecturer, "Digital-Logic-Design" *09/2014-12/2014*
ECE department, Northeastern University, Boston, MA, USA
- Taught theoretical aspects of digital design as well as Verilog-HDL programming
- Students were able to design a calculator on Xilinx Spartan FPGAs (over 40 students)
- Received a very good student evaluation (4.1 out of 5.0 for teaching effectiveness)

Guest Lecturer, "Microprocessor-Based Design" *02/2014-04/2014*
ECE department, Northeastern University, Boston, MA, USA
- Lectured on the architecture of ADI Blackfin DSP processors
- Received excellent student evaluation (4.7 out of 5.0 for teaching effectiveness)

Teaching Assistant, "High-Level Design of Hardware / Software Systems" *09/2011-12/2011*
ECE Department, Northeastern University, Boston, MA, USA

Teaching Assistant, "Optimization Methods" *09/2010-12/2010*
ECE Department, Northeastern University, Boston, MA, USA

Instructor/Lecturer, "Computer Architecture" and "Digital-Logic-Design" *09/2008-05/2010*
School of Engineering, Shariaty College, Tehran, Iran
- Designed and developed the syllabus, lecture materials and lab assignments
- Worked with over 150 undergraduate students over two years

Advising / Technical Supervision

I have supervised **3 Ph.D.** and **8 M.Sc.** students. The students (except Amir Momeni) are advised by Prof. Gunar Schirner.

Ph.D. Students

- Nasibeh Teimouri, topic: heterogeneous architecture for accelerator-based design
- Amir Momeni, topic: bridging architecture and OpenCL programming abstractions for FPGA devices (advised by Prof. David Kaeli)
- Mohammad Khavari Tavana: topic: high-performance low-power accelerator architecture for Deep Convolutional Neural Networks (D-CNNs)

Current M.Sc. Students

- Chulian Zhang, topic: divergence-aware Warps scheduler to enhance GPUs performance
- Pritpal Bains, topic: design automation for architecting at function-level granularity
- Shankar Kartik, topic: Function-Set-Architecture (FSA) explorer for market-oriented MPSoCs
- Wenyu Kui, topic: multi-core software development for object tracking vision flow
- Laura Clark, topic: a novel architecture for 2D pyramid-based vision processing

Alumni M.Sc. Students

- Majid Sabbagh, 08/2015, design and analysis of low power heterogeneous real-time embedded vision applications, PhD student at Northeastern University
- Fan Xu, 08/2015, HW/SW co-design solution for component-labeling object detection, HP
- Chenyan Liu, 08/2014, design and implementation of real-time vision filters, EMC

Industrial Experience

CPU R&D Intern *09/2012 - 12/2012*

Qualcomm Inc., Raleigh, NC, USA

- Optimized the front-end of ARM cores for power and performance efficiency
- Manager: David Hansquine, Email: *dhansqui@qualcomm.com*

Invited Talks

"Escaping the flexibility and efficiency trade-off through algorithm/architecture co-design"
University of Texas, Dallas, TX, USA *04/2016*

"Heterogeneous many-core architectures for embedded deployment of streaming applications"
Sate University of New York (SUNY), Binghamton, NY, USA *03/2016*

"Heterogeneous many-core architectures for embedded deployment of streaming applications"
University of Massachusetts, Boston, MA, USA *03/2016*

"Heterogeneous many-core architectures for embedded deployment of streaming applications"
University of North Carolina, Charlotte, NC, USA *02/2016*

"High-performance power-efficient embedded vision computing"
Worcester Polytechnic Institute (WPI), Worcester, MA, USA *01/2016*

"High-performance power-efficient embedded vision computing"
University of Massachusetts, Boston, MA, USA *11/2015*

"High-performance power-efficient solutions for embedded vision"
MathWorks, Natick, MA, USA *09/2014*

"System-level solutions for early architecture exploration"
Analog Devices Inc. (ADI), Norwood, MA, USA *10/2013*

"Investigating the cost and benefits of trace cache for ARM cores"
Qualcomm Inc., Raleigh, NC, USA *11/2012*

"Methodologies for system-level design space exploration and automatic refinement"
Qualcomm Inc., Raleigh, NC, USA *09/2012*

Honors and Awards

Top 10 most downloaded articles	*IET Computers & Digital Techniques, June 2015*
DAC PhD forum most popular poster presentation	*ACM SIGDA, 2015*
DAC PhD forum travel grant	*ACM SIGDA, 2015*
Best Paper Runner-up	*Application-Specific Architectures and Processors (ASAP,) 2014*
Young student travel grant	*Design Automation Conference (DAC), 2012*
$125K support on my research in embedded vision computing	*Analog Devices Inc. (ADI)), 2011*
Research Assistantship award	*Northeastern University, 2010*
Ranked 3rd across computer engineering M.Sc. students	*Sharif University of Technology, 2008*
Ranked 18th among 10000 candidates in Iran national exam for CE graduate studies	*2006*

Professional Service

Organizing Committee

- Session chair, Great Lakes Symposium on VLSI (GLS-VLSI) *2016*
- Publicity chair, International Embedded Systems Symposium (IESS) *2015*

Technical Program Committee Member

- International Conference on Great Lakes Symposium on VLSI (GLS-VLSI) *2016*
- 9th Workshop on Graphics Processor for General Purpose Processing (GPGPU-9) *2016*
- International Embedded Systems Symposium (IESS) *2015*

Journal / Book Chapter Reviewer

- ACM Transactions on Embedded Computer Systems (TECS) *2015, 2016*
- ACM Transactions on Design Automation of Electronic Systems (TODAES) *2015, 2016*
- ACM Transactions on Architecture and Code optimization (TACO) *2014, 2015*
- IEEE Transaction on VLSI systems (TVLSI) *2013, 2016*
- Elsevier Journal of Microprocessors and Microsystems (MICPRO) *2015*
- Elsevier Journal of Parallel and Distributed Computing (JPDC) *2015*
- Springer Handbook of HW/SW Co-design *2016*

Conference External Reviewer

- Design Automation Conference (DAC) *2013, 2014, 2015, 2016*
- Design, Automation and Test in Europe (DATE) *2013, 2014, 2015, 2016*
- Conference on HW/SW Co-Design and System Synthesis (CODES+ISSS) *2011, 2012, 2013*
- International Conference on Embedded Computer Systems: Architecture, Modeling and Simulation (SAMOS XV) *2015*
- International Embedded Systems Symposium (IESS) *2015*

References

Prof. Gunar Schirner
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Prof. Rainer Dömer
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