1) SYSTEM-LEVEL CAD

1.1 System Design:
- System-level specification, modeling, and simulation
- System design flows and methods
- HW/SW co-design, co-simulation, co-optimization, and co-exploration
- HW/SW platforms for rapid prototyping
- System design case studies and applications
- System-level issues for 3D integration
- Micro-architectural transformation
- Memory architecture and system synthesis
- System communication architecture
- Network-on-chip design methodologies and CAD

1.2 Embedded Systems Hardware:
- Multi-core/multi-processors systems
- HW/SW co-design for embedded systems
- Static and dynamic reconﬁgurable architectures
- Memory hierarchies and management
- System-level consideration of custom storage architectures
- Flash, phase change memory, STT-RAM, etc.
- Application-speciﬁc instruction-set processors (ASIPs)
- Hardware-based security (CAD for PUF’s, RNG, AES etc.)
- Detection and prevention of hardware Trojans
- Side-channel attacks, fault attacks and countermeasures
- Split manufacturing for security

1.3 Embedded Systems Software:
- Real-time software and operating systems
- Middleware and virtual machines
- Timing analysis and WCET
- Programming models for multi-core systems
- Proﬁling and compilation techniques
- Design exploration, synthesis, validation, veriﬁcation, and optimization
- System software security techniques

1.4 Dark Silicon and Power/Thermal Considerations
- Power and thermal estimation, analysis, optimization, and management
- Energy- and thermal-aware application mapping and scheduling
- Energy- and thermal-aware dark silicon system design and optimization
- Run-time management for the dark silicon

1.5 Design Issues for Heterogeneous Computing
- Hardware-software partitioning of workloads
- High-level synthesis for heterogeneous computing
- Power/performance analysis of heterogeneous platforms
- Programming environment of heterogeneous computing
- Acceleration techniques including GPGPU, FPGA and specialized ASIC’s
- Application driven heterogeneous platforms for big data, machine learning etc.

2) SYNTHESIS, VERIFICATION, AND PHYSICAL DESIGN

2.1 High-Level, Behavioral, and Logic Synthesis and Optimization:
- High-level/Behavioral/Logic synthesis
- Technology-independent optimization and technology mapping
- Functional and logic timing ECO
- Resource scheduling, allocation, and synthesis
- Interaction between logic synthesis and physical design

2.2 Validation, Simulation, and Veriﬁcation:
- High-level/Behavioral/Logic modeling and validation
- High-level/Behavioral/Logic simulation
- Formal, semi-formal, and assertion-based veriﬁcation
- Equivalence and property checking
- Emulation and hardware simulation/acceleration
- Post-silicon functional validation

2.3 Cell-Library Design, Partitioning, Floorplanning, Placement:
- Cell-library design and optimization
- Transistor and gate sizing
- High-level physical design and synthesis
- Estimation and hierarchy management
- 2D and 3D partitioning, ﬂoorplanning, and placement
- Post-placement optimization
- Buffer insertion and interconnect planning

2.4 Network Synthesis, Routing, and Post-Layout Optimization and Veriﬁcation:
- 2D and 3D clock network synthesis
- 2D and 3D global and detailed routing
- Package-/Board-level routing and chip-package-board co-design
- Post-layout/silicon optimization

3) SOC ANALYSIS, SIMULATION AND TESTING

3.1 Design for Manufacturability:
- Process technology characterization, extraction, and modeling
- CAD for design/manufacturing interfaces
- CAD for reticle enhancement and lithography-related design
- Variability analysis and statistical design and optimization
- Yield estimation and design for yield
- Physical veriﬁcation and design rule checking

3.2 Design for Reliability:
- Analysis and optimization for device-level reliability issues (stress, aging effects, ESD, etc.)
- Analysis for interconnect reliability issues (electromigration, thermal, etc.)
- Reliability issues related to soft errors
- Design for resilience and robustness

3.3 Testing:
- Digital fault modeling and simulation
- Delay, current-based, low-power test
- ATPG, BIST, DFT, and compression
- Memory test and repair
- Core, board, system, and 3D IC test
- Post-silicon validation and debug
- Analog, mixed-signal, and RF test

3.4 Timing, Power Networks and Signal Integrity:
- Deterministic and statistical static timing analysis and optimization
- Power and leakage analysis and optimization
- Circuit and interconnect-level low power design issues
- Power/ground network analysis and synthesis
- Signal integrity analysis and optimization

3.5 CAD for RF/analog, Multi-Domain Modeling and Interconnect
- CAD for analog, mixed-signal and RF
- CAD for mixed-domain (semiconductor, nanoelectronic, MEMS, and electro-optical) devices, circuits, and systems
- CAD for nanophotonics
- Device, interconnect and circuit extraction and simulation
- Package modeling and analysis
- EM simulation and optimization
- Behavior modeling of devices and interconnect
- Modeling of complex dynamical systems (molecular dynamics, ﬂuid dynamics, computational ﬁnance, etc.)

4) CAD FOR EMERGING TECHNOLOGIES AND APPLICATIONS

4.1 Biological Systems and Bio-Electronics:
- CAD for biological computing systems
- CAD for synthetic biology
- Tools, methods and hardware for systems and computational biology
- CAD for bio-electronic devices, bio-sensors, MEMS, and systems

4.2 Nanoscale and Post-CMOS Systems:
- New device structures and process technologies
- New memory technologies (ﬂash, phase change memory, STT-RAM, memristor, etc.)
- Nanotechnologies, nanowires, nanotubes, graphene, etc.
- Quantum computing
- Optical devices and communication
- CAD for bio-inspired and neuromorphic systems

4.3 CAD for Cyberphysical Systems:
- CAD for internet-of-things and sensor networks
- CAD for automotive systems and power electronics
- Analysis and optimization of data centers
- CAD for display electronics
- Green computing (smart grid, energy, solar panels, etc.)
Deadline for Electronic Submission of Abstracts: 
**FRIDAY, APRIL 17, 2015**
5:00PM PACIFIC DAYLIGHT TIME (GMT -7)

**SUBMISSION DETAILS**

Paper submissions must be made through the online submission system at the ICCAD web site: [https://www.iccad.com](https://www.iccad.com). Regular papers will be reviewed as finished papers; preliminary submissions will be at a disadvantage.

Authors are asked to submit their work in two stages. In stage one (abstract submission), a title, abstract, and a list of all co-authors must be submitted via the ICCAD web submission site. In stage two (paper submission), the paper itself is submitted. Authors are responsible for ensuring that their paper submission meets all guidelines, and that the PDF is readable.

**DEADLINE FOR ABSTRACT SUBMISSIONS**
The submission abstract deadline is 5:00 pm Pacific Daylight Time (GMT -07:00), Friday April 17, 2015. No abstract submissions will be possible after this deadline.

Deadline for Paper Submissions The submission paper deadline is 5:00 pm Pacific Daylight Time (GMT -07:00), Friday April 17, 2015.

We always have several authors contact the ICCAD office asking for a deadline extension. Due to the limited review cycle, NO extensions are granted for ANY reason.

**REGULAR PAPER SUBMISSIONS**

- All papers must be in PDF format only, with savable text.
- Each paper must be no more than 8 pages (including the abstract, figures, tables, and references), double-columned, 9pt or 10pt font.
- Your submission must not include information that serves to identify the authors of the manuscript, such as name(s) or affiliation(s) of the author(s), anywhere in the manuscript, abstract, or in the embedded PDF data. References and bibliographic citations to the author(s) own published works or affiliations should be made in the third person.
- Submissions not adhering to these rules, or determined to be previously published (this includes pre-prints publicly available on personal or other websites, such as arXiv, or publicly available internal memoranda with author names divulged) or simultaneously submitted to another conference, or journal, will be summarily rejected. Internal memoranda with full content not publicly available, and with author names not divulged, may be submitted.

**IMPORTANT:** Final camera-ready versions must be identical to the submitted papers with the following exceptions; inclusion of author names/affiliation, correction of identified errors, addressing reviewer-demanded changes. No other modifications of any kind are allowed including modification of title, change of the author list, reformatting, restyling, rephrasing, removing figures/results/text, etc. The TPC Chairs reserve the right to finally reject any manuscripts not adhering to these rules. A report detailing all the revisions made must be submitted together with the final camera-ready manuscript once any revision is conducted.

**TEMPLATES**

Paper templates are available at the ICCAD website; authors are recommended to format their papers based on the templates.

**NOTIFICATION OF ACCEPTANCE**

Authors will be notified of acceptance on or before Monday, June 22, 2015. Final paper guidelines will be sent at that time.
Call for Workshop, Tutorial, Special Session, Panel and Keynote Proposals, all due Thursday, April 30, 2015.

WORKSHOP PROPOSALS
ICCAD provides a vibrant and supportive environment for small-to-medium-sized affiliated workshops. Typical workshops are one-day events on the Thursday of ICCAD, with ICCAD providing all logistical support (registration, lunch, room bookings, hotel, pre-conference financials, etc.) All workshop proposals should be sent to David Pan, Workshop Chair, at dpan@ece.utexas.edu.

TUTORIAL PROPOSALS
All ICCAD tutorials are embedded in the main technical program and free to conference attendees, providing value to attendees and a good audience for presenters. Typical tutorials run 1.5-2 hours, although longer tutorials (consisting of two session blocks of 1.5-2 hours each) may be considered. Tutorial suggestions should not exceed two pages, should describe the topic and intended audience, and must include a list of suggested participants with biographical data. Proposals should focus on the state-of-the-art in a specific area of broad interest amongst ICCAD attendees. All tutorial proposals should be sent to Iris Bahar, Tutorial and Special Session Chair, at iris_bahar@brown.edu.

SPECIAL SESSION PROPOSALS
Special Sessions typically run 1.5-2 hours. Special session proposals should focus on in-depth treatment on a topic of timely interest to the ICCAD audience. Special session proposals should not exceed two pages, should describe the topic and intended audience, and must include a list of suggested participants with biographical data. All special session proposals should be sent to Iris Bahar, Tutorial and Special Session Chair, at iris_bahar@brown.edu.

PANEL PROPOSALS
Panel suggestions should not exceed two pages, should describe the topic and intended audience, and should include a list of suggested participants. Panel suggestions must include a bulleted outline of covered topics. All panel proposals should be sent to Sri Parameswaran, Technical Program Vice-Chair at sridevan@cse.unsw.edu.au.

KEYNOTE PROPOSALS
Keynote proposals should include descriptions of suggested keynote speakers, and the importance of the speech to the ICCAD audience. All keynote proposals should be sent to Diana Marculescu, General Chair, at dianam@cmu.edu.

ICCAD reserves the right to restructure all panel, special session, and tutorial proposals.

IF YOU NEED ASSISTANCE, PLEASE CONTACT THE APPROPRIATE COMMITTEE MEMBERS:

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Diana Marculescu, dianam@cmu.edu

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Frank Liu, frankliu@us.ibm.com

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Tutorial and Special Session Chair:
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Workshop Chair:
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